

What is claimed is:

- 1 1. An integrated circuit, comprising:
 - 2 a pulse generator adapted to generate a pulsed signal;
 - 3 a cycle counter adapted to count cycles of said pulsed signal;
 - 4 one or more repairable circuit elements; and
 - 5 a repair processor adapted to repair a repairable circuit element when said cycle
 - 6 counter reaches a pre-determined cycle count.
- 1 2. The integrated circuit of claim 1, wherein said repair processor, replaces said repairable
- 2 circuit element with a redundant circuit element having the same function as said
- 3 repairable circuit element.
- 1 3. The integrated circuit if claim 1, wherein said pulsed signal is a clock signal and said
- 2 repairable circuit element is responsive to said clock signal.
- 1 4. The integrated circuit of claim 1, further including a memory circuit adapted to store a
- 2 cycle count of the number of cycles counted since an initial power up and to resume
- 3 counting from said stored cycle count after a power down/power up cycle of said
- 4 integrated circuit.

1 5. The integrated circuit of claim 1, wherein:

2 said cycle counter is adapted to generate a trigger signal when said predetermined

3 cycle count is reached; and

4 said repair processor is adapted to receive said trigger signal and affect a repair of

5 said repairable circuit element when said trigger signal is received.

1 6. The integrated circuit of claim 5, wherein said trigger signal comprises a subset of a set

2 of bits encoding a current cycle count of said cycle counter.

1 7. The integrated circuit of claim 1, wherein said repairable circuit element is selected

2 from the group consisting of a digital circuit, an analog circuit, a memory circuit, a latch,

3 a logic gate, a group of logic gates, an individual devices, a transistor, a diode, a resistors,

4 a capacitor, an inductor and a wire.

1 8. The integrated circuit of claim 1, wherein said repairable circuit element is

2 implemented in a field programmable gate array and said repair processor programs a

3 replacement of selected gates of said field programmable gate array with previously

4 unused gates of said field programmable gate array.

1 9. The integrated circuit of claim 1, further including a fuse bank for storing information

2 used to implement a repair of said repairable circuit element.

1 10. The integrated circuit of claim 1, wherein in said repair processor is adapted to
2 perform multiple repairs by repairing previously repaired repairable circuit elements.

1 11. The integrated circuit of claim 1, further including:
2 a redundant cycle counter; and
3 wherein said repair processor is adapted to replace said cycle counter with said
4 redundant cycle counter when said cycle counter reaches a fixed cycle count.

1 12. A method of preemptively repairing an integrated circuit, comprising:

2 (a) a pulse generated adapted to generate a pulsed signal;

3 (b) providing a cycle counter adapted to count cycles of said pulsed signal;

4 (c) providing one or more repairable circuit elements; and

5 (d) providing a repair processor adapted to repair a repairable circuit element

6 when said cycle counter reaches a pre-determined cycle count.

1 13. The method of claim 12, wherein said step (d) includes replacing said one or more
2 repairable circuit element with a redundant circuit element having the same function as
3 said repairable circuit element.

1 14. The method if claim 12, wherein said pulsed signal is a clock signal and said
2 repairable circuit element is responsive to said clock signal.

1 15. The method of claim 12, further including a memory circuit adapted to store a cycle
2 count of a number of cycles counted since an initial power up and to resume counting
3 from said stored cycle count after a power down/power up cycle of said integrated circuit.

1 16. The method of claim 12, wherein:
2 said cycle counter is adapted to generate a trigger signal when said predetermined
3 cycle count is reached; and

4 said repair processor is adapted to receive said trigger signal and affect a repair of
5 said repairable circuit element when said trigger signal is received.

1 17. The method of claim 16, wherein said trigger signal comprises a subset of a set of bits
2 encoding a current cycle count of said cycle counter.

1 18. The method of claim 12, wherein said repairable circuit element is selected from the
2 group consisting of a digital circuit, an analog circuit, a memory circuit, a latch, a logic
3 gate, a group of logic gates, an individual device, a transistor, a diode, a resistor, a
4 capacitor, an inductor and a wire.

1 19. The method of claim 12, wherein said repairable circuit element is implemented in a
2 field programmable gate array and said repair processor programs a replacement of
3 selected gates of said field programmable gate array with previously unused gates of said
4 field programmable gate array.

1 20. The method of claim 12, further including providing a fuse bank for storing
2 information used to implement a repair of said repairable circuit element.

1 21. The method of claim 12, wherein in said repair processor is adapted to perform
2 multiple repairs by repairing previously repaired repairable circuit elements.

- 1 22. The method of claim 12, further including:
 - 2 providing a redundant cycle counter; and
 - 3 said repair processor automatically replacing said cycle counter with said
- 4 redundant cycle counter when said cycle counter reaches a fixed cycle count.

1 23. A method for designing a repairable integrated circuit, comprising:

2 generating an integrated circuit design from a design library of circuit elements;

3 simulating said integrated circuit design and generating a switching report for

4 circuit elements of said integrated circuit design;

5 selecting a circuit element responsive to a pulsed signal of said integrated circuit

6 design based on said switching report;

7 selecting a repairable circuit element from said design library, said repairable

8 circuit element having the same function as said selected circuit element and allowing

9 multiple connection paths; and

10 inserting said selected repairable circuit element, a cycle counter adapted to count

11 cycles of said pulsed signal and repair processor adapted to repair said repairable circuit

12 element when said cycle counter reaches a pre-determined value into said integrated

13 circuit design.

1 24. The method of claim 23, wherein said switching report indicates a number of state

2 toggles of each selected circuit element performed during said simulation.

1 25. The method of claim 23, wherein said repairable circuit element is selected from the

2 group consisting of a digital circuit, an analog circuit, a memory circuit, a latch, a logic

3 gate, a group of logic gates, an individual device, a transistors, a diode, a resistor, a

4 capacitor, an inductors and a wire.

- 1 26. The method of claim 23, wherein said repairable circuit element is implemented in a
- 2 field programmable gate array having spare gates and said repair processor includes a
- 3 circuit for programming said field programmable array to use programmed spare gates in
- 4 place of the gates originally programmed to implement said repairable circuit element.

1 27. A computer system comprising a processor, an address/data bus coupled to said
2 processor, and a computer-readable memory unit adapted to be coupled to said processor,
3 said memory unit containing instructions that when executed by said processor implement
4 a method for a method for designing a repairable integrated circuit, said method
5 comprising the computer implemented steps of:
6 generating an integrated circuit design from a design library of circuit elements;
7 simulating said integrated circuit design and generating a switching report for
8 circuit elements of said integrated circuit design;
9 selecting a circuit element responsive to a pulsed signal of said integrated circuit
10 design based on said switching report;
11 selecting a repairable circuit element from said design library, said repairable
12 circuit element having the same function as said selected circuit element and allowing
13 multiple connection paths; and
14 inserting said selected repairable circuit element, a cycle counter adapted to count
15 cycles of said pulsed signal and repair processor adapted to repair said repairable circuit
16 element when said cycle counter reaches a pre-determined value into said integrated
17 circuit design.

1 28. The system of claim 27, wherein said switching report indicates a number of state
2 toggles of said circuit element performed during said simulation.

1 29. The system of claim 27, wherein said repairable circuit element is selected from the
2 group consisting of a digital circuit, an analog circuit, a memory circuit, a latch, a logic
3 gate, a group of logic gates, an individual device, a transistor, a diode, a resistor, a
4 capacitor, an inductor and a wire.

1 30. The method of claim 27, wherein said repairable circuit element is implemented in a
2 field programmable gate array having spare gates and said repair processor includes a
3 circuit for programming said field programmable array to use programmed spare gates in
4 place of the gates originally programmed to implement said repairable circuit element.